GOODRAM SSD
M.2 2280 E13T 3D TLC
DATASHEET

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REVISION HISTORY

VERSION	CHANGES	DATE
1.0	Initial release	26.11.2021

TABLE OF CONTENTS

PRODUCT OVERVIEW

- **Capacity**
  - 128GB - 512GB
- **Form Factor**
  - M.2 2280-S2-M
- **Interface**
  - PCIe Gen3 x4
- **Complience**
  - NVMe 1.3
  - PCI Express Base 3.1
- **Flash Interface**
  - Flash type: Micron 3D TLC
  - Up to 2pcs of BGA 132 flash
- **Performance** Note1
  - Read: up to 2400 MB/s
  - Write: up to 1900 MB/s
- **Power Consumption** Note2
  - Active < 2800 mW
  - Idle < 30 mW
  - PS4 L1.2 < 5 mW
- **Controller**
  - Phison PS5013-E13T
- **MTBF**
  - More than 1,500,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-provisioning
  - Firmware update
- **Power Management**
  - PS0/PS1/PS2/PS3/PS4
  - Support APST
  - Support ASPM
  - Support L1.2
- **Temperature Range** Note3
  - Operational: 0 ~ +70°C
  - Storage: -40°C ~ +85°C
- **RoHS compliant**

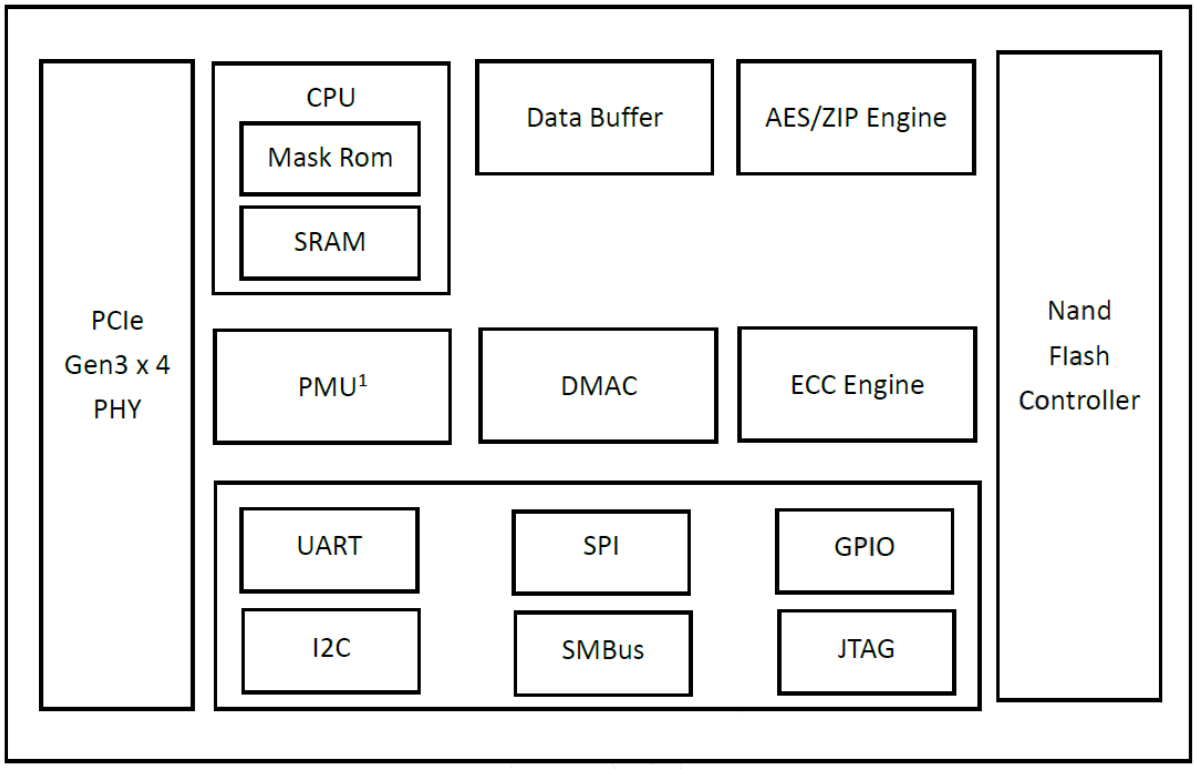
Notes:
1. Measured by CrystalDiskMark v3.0
2. Please see “Power Consumption” for details.
3. According to standards IEC-60068-2-1/2/14/38

PRODUCT DETAILS

GENERAL DESCRIPTION

GOODRAM M.2 2280 E13T delivers all the advantages of flash disc technology with PCIe Gen3 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. The capacity could provide a wide range up to 2048GB. Meanwhile, the power consumption is much lower than traditional Hard Drives.

CONTROLLER BLOCK DIAGRAM



PS5013-E13T Controller Block Diagram

FLASH MANAGEMENT

GOODRAM M.2 2280 modules utilizes all the state of art technologies to ensure full reliability until the TBW parameter is reached. These technologies include:

Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data, therefore M.2 2280 applies the LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media. Product has advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. We implement an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) is improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgraded when new features are added, compatibility issues are fixed or read/write performance gets improved.

Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. M.2 is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

ADDITIONAL FEATURES

Advanced Device Security Features (Secure Erase, Crypto Erase, Physical Presence SID)

Secure Erase is a standard NVMe command and will write all “0x00” to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings. Crypto Erase is a feature that erases all data of an OPAL-activated SSD or a “SED” Security-Enabled Disk) drive by resetting the cryptographic key of the disc. Once the disc is modified, the previously encrypted data will become useless, achieving the purpose of data security. PSID is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when OPAL-activated SSD supports PSID revert feature.

PERFORMANCE AND POWER CONSUMPTION

Capacity	Flash Structure	Performance		Power Consumption	
		CrystalDiskMark		Read (mW)	Write (mW)
		Read (MB/s)	Write (MB/s)		
128GB	128GBx1	2300	1200	2150	2000
256GB	128GBx2	2300	1200	2150	2000
512GB	256GBx2	2400	1800	2300	2400

NOTES:

1. The performance was measured using CrystalDiskMark host.
2. Samples were built using Micron 3D TLC NAND flash.
3. Performance and power consumption may differ according to flash configuration, SDR configuration, and platform.
4. The table above is for reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration.

SUPPLY VOLTAGE

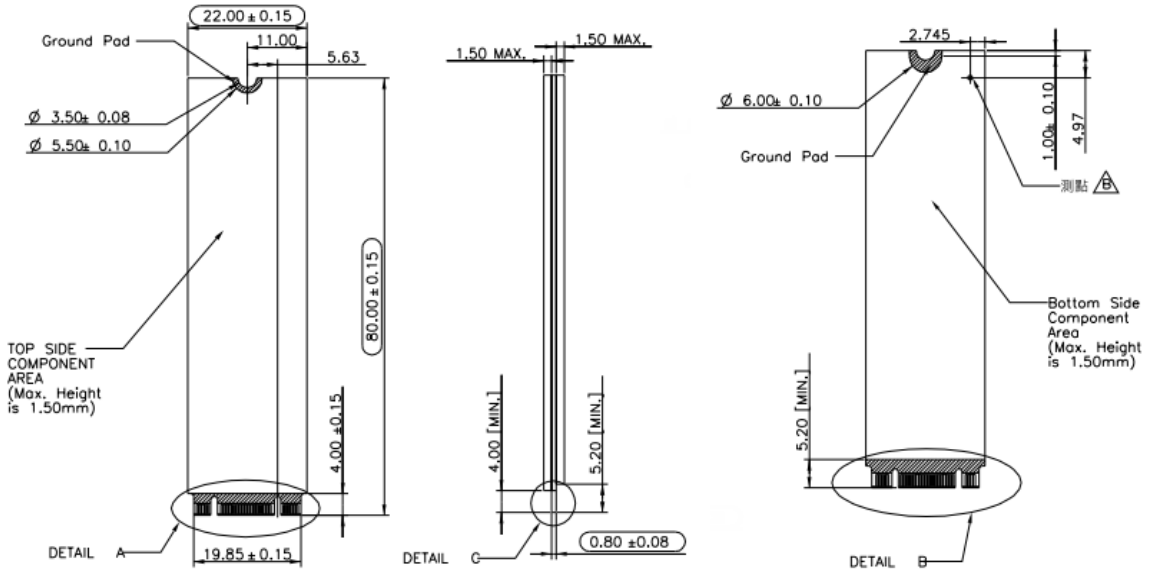
PARAMETER	RATING
Operating voltage	3.3V +/- 5%

PRODUCT ORDERING INFORMATION

PN	Type	Capacity	Technology	Temp range	Grade
RUSM8T128P3SB-PE3MCD	M.2	128GB	3D TLC	0~70°C	Silver
RUSM8T256P3SB-PE3MCD	M.2	256GB	3D TLC	0~70°C	Silver
RUSM8T512P3SB-PE3MCD	M.2	512GB	3D TLC	0~70°C	Silver

PHYSICAL DIMENSION

Dimension: 80mm(L) x 22mm(W) x 3.75mm(H)



PIN ASSIGNMENT AND DESCRIPTIONS

Pin	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull -up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull -up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull -up on platform; Active low.
45	GND	Ground
46	N/C	No connect

47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No connect
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	NC	CONFIG_1 = No connect
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	CONFIG_2 = Ground

NVMe Command List

Admin Commands

Opcode	Command Description	Opcode	Command Description
00h	Delete I/O Submission Queue	0Ah	Get Features
01h	Create I/O Submission Queue	0Ch	Asynchronous Event Request
02h	Get Log Page	0Dh	Namespace Management
04h	Delete I/O Completion Queue	10h	Firmware Active
05h	Create I/O Completion Queue	11h	Firmware Image Download
06h	Identify	14h	Device Self-test
08h	Abort	15h	Namespace Attachment
09h	Set Features	18h	Keep Alive

STANDARDS & REFERENCES

The following table is to list out the standards that have been adopted for designing the product.

STANDARD USED	ACRONYM/SOURCE
RoHS	Restriction of Hazardous Substances Directive; please contact us for further information.
M.2	http://www.pcisig.com
PCI Express Base 3.0	https://www.pcisig.com/specifications/pciexpress/base3/
NVM Express Specification Rev.1.3	http://www.nvmexpress.org/
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a
CE	Consumer electronics certification; please contact us for further information.

SAFETY PRECAUTIONS

Do not bend, crush, drop, or place heavy objects on top of the Product. Do not use tweezers, pliers or similar items that could damage the Product. Take particular care when inserting or removing the Product. Stop using the Product when the Product does not work properly. Failure to follow these instructions could result in fire, damage to the Product and/or other property, and/or personal injury including burns and electric shock.

Keep out of reach of small children. Accidental swallowing may cause suffocation or injury. Contact a doctor immediately if you suspect a child has swallowed the Product.

Do not directly touch the interface pins, put them in contact with metal, strike them with hard objects or cause them to short. Do not expose to static electricity.

Do not disassemble or modify the Product. This may cause electric shock, damage to the Product or fire.

NOTES ON USAGE

The Product contains nonvolatile semiconductor memory. Do not use the Product in accordance with a method of usage other than that written in the manual. This may cause the destruction or loss of data.

To protect against accidental data loss, you should back up your data frequently on more than one type of storage media. Wilk Elektronik S.A. assumes no liability for destruction or loss of data recorded on the Card for any reason.

When used over a long period of time or repeatedly, the reading, writing and deleting capabilities of the Product will eventually fail, and the performance speed of the Product may decrease below the original speed specific to the Product's applicable class.

If the Product is to be transferred or destroyed, note that the data it contained may still be recoverable unless it is permanently deleted by third-party deletion software or similar means beforehand.

Product is intended for use in general electronics applications and selected industrial applications and any other specific applications as expressly stated in this document. Product is neither intended nor warranted for use in equipment or systems where failure may cause loss of human life, bodily injury, serious property damage or serious public impact (“Unintended Use”). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment or equipment used to control combustions or explosions. Do not use Product for Unintended Use unless specifically permitted in this document.

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